Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.143”**

**.152”**

**SOURCE**

**GATE**

**Top Material: Al**

**Backside Material: AgTiNi**

**Bond Pad Size: G = .038 x .051” S = .040 x .060”**

**Backside Potential: DRAIN**

**Mask Ref: GEN 3**

**APPROVED BY: DK DIE SIZE .143” X .152” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC034**

**DG 10.1.2**

#### Rev B, 7/1